A Novel Quick Response of RBCOT With VIC Ripple for Buck Converter

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Abstract—A novel quick response of ripple-based constant ontime with virtual inductor current ripple for Buck converter is proposed in this paper. The concept uses the capacitor and the resistor in a series to filter out the output voltage at load transient to dynamically change the width of on-time to prevent the $V_{\rm out}$ from dropping markedly. Finally, 12-V input voltage, 3.3-V output voltage, and 60-W output power with the novel quick response circuit for the IC of the proposed Buck converter are implemented to verify its viability and superiority.

Index Terms—Quick response, ripple-based constant on-time (RBCOT), virtual inductor current (VIC) ripple.

I. Introduction

WITCHING converters are very popular in electronic devices [1]–[11]. The ripple-based constant on-time (RBCOT) control scheme is widely used in the improvement of light-load efficiency because it can reduce switching frequency and save switching related loss [1], [13]–[22]. It also has a faster transient response than traditional voltage mode control [1], [14]–[17]. Fig. 1 shows the circuit diagram of the conventional RBCOT control for Buck converter. S1 and S2 are the switches, L is the output inductor, and R_{CO} is the equivalent series resistance (ESR) of the output capacitor C_O . The diagram shows that the output voltage ripple includes inductor current information. The current source $I_{\rm out}$ is the output load, and $R_{\rm d1}$ and $R_{\rm d2}$ are the feedback resistors to determine output voltage. The feedback voltage $V_{\rm fb}$ and the reference voltage $V_{\rm ref}$ are built inside the IC.

In the conventional RBCOT topology, the absence of virtual inductor current (VIC) ripple to add in the feedback voltage [1],

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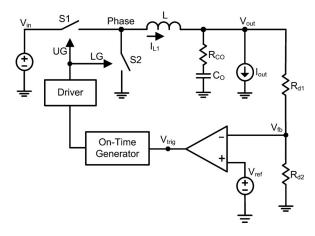


Fig. 1. Circuit diagram of the conventional RBCOT control for Buck converter.

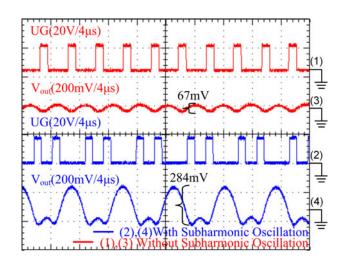


Fig. 2. Comparison of the subharmonic oscillations among the experimental waveforms of the conventional RBCOT for Buck converter.

[23]–[26], which is the integration of ac ripple of the inductor current, causes the time-delay effects in the loop. Thus, this control scheme suffers from instability, due to the subharmonic oscillations in the converter when using low ESR capacitors, such as ceramic capacitors [1], [27]–[31]. The present control scheme in this study does not entirely make use of ceramic capacitors.

Fig. 2 shows a comparison of the subharmonic oscillations among the experimental waveforms of the conventional RBCOT for Buck converter [1], [24]–[27]. The experimental waveforms include the upper gate (UG) and the $V_{\rm out}$ signals, both with and without subharmonic oscillations. The subharmonic oscillations

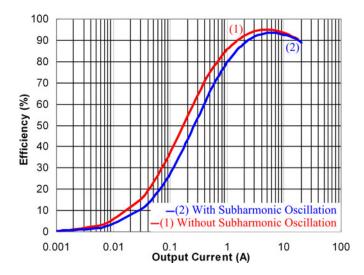


Fig. 3. Comparison of the efficiency among the experimental results of the subharmonic oscillations of the conventional RBCOT for Buck converter.

can directly cause very high output voltage. The output voltage with subharmonic oscillation is 284 mV higher than that without subharmonic oscillations (67 mV), indicating a difference of about four times the experimental waveforms. On the other hand, the switching loss with subharmonic oscillations is larger than that without subharmonic oscillations.

Fig. 3 shows a comparison of the efficiency among the experimental results of the subharmonic oscillations of the conventional RBCOT for Buck converter [1], [24]–[27]. The subharmonic oscillations can directly cause large switching loss. The difference between the efficiency of the converter that has subharmonic oscillations (43.45%) and the one without subharmonic oscillations (54.4%) is about 11% at a light load of 0.2 A. However, the efficiency of that with subharmonic oscillations is very close to that without subharmonic oscillations at a heavy load of 20 A, because the conduction loss is a major factor that affects the efficiency in this condition.

II. RIPPLE-BASED CONSTANT ON-TIME CONTROL WITH VIRTUAL INDUCTOR CURRENT RIPPLE

Fig. 4 shows the circuit structure of the RBCOT control with VIC ripple for Buck converter. The use of a VIC ripple is proposed to alleviate the instability problem because it enhances the effect of the ESR voltage ripple in the feedback voltage. This scheme provides better system stability, especially in all ceramic output capacitors, which normally have relatively low ESR values.

In a VIC ripple generator, the phase voltage is filtered by low-pass filter $R_{\rm LPF}$ and $C_{\rm LPF}$. The corner frequency of the low-pass filter is designed close to the resonant frequency [1]. Then, the dc value of $V_{\rm CLPF}$ is removed by the dc value extractor to generate a VIC ripple. The VIC ripple is added in the feedback voltage $V_{\rm fb}$ to enhance the ESR voltage ripple, as shown in Fig. 5 [1]. This control structure can provide better system stability without sensing current information or adding extra components. The

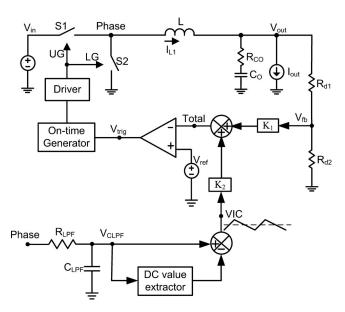


Fig. 4. Circuit structure of the RBCOT control with virtual inductor current ripple for Buck converter.

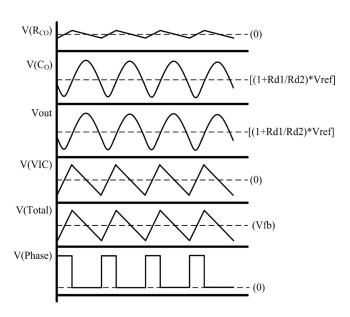


Fig. 5. Waveforms of virtual inductor current ripple generator.

phase voltage is built inside the IC; thus, it does not need an extra IC pin for implementation.

Fig. 6 shows the on-time generator circuit of the RBCOT control with VIC ripple for Buck converter. The TON pin is in one of the IC, and the resistor R_1 can be placed between the TON pin and the input voltage to determine the width of on-time. The output voltage $V_{\rm out}$ needs to be sensed to limit the voltage from capacitor C_1 by (1). The output voltage $V_{\rm out}$ divided by the input voltage $V_{\rm in}$ is a duty cycle, and R_1 , C_1 , and C_1 are constant values, like the switching period C_1 , by (2). C_2 is a gain of current-controlled current source. Even if the input voltage C_1 and the output voltage C_2 are changed, the system still maintains the same switching frequency. Thus, this control

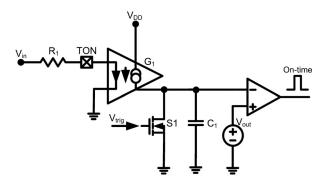


Fig. 6. On-time generator circuit of the RBCOT control with VIC ripple for Buck converter.

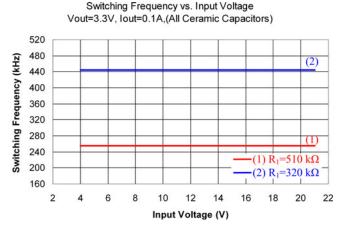


Fig. 7. Experimental results of the switching frequency versus the input voltage for CFCOT.

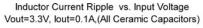
is called constant frequency constant on-time (CFCOT) [23]

$$T_{\rm ON} = \frac{V_{\rm out}}{V_{\rm in}} \times \frac{R_1 \cdot C_1}{G_1} \tag{1}$$

$$T_{\rm ON} = \frac{V_{\rm out}}{V_{\rm in}} \times T_S. \tag{2}$$

CFCOT is different from the conventional COT control circuit because it avoids the generation of the same width of on-time at the high-output voltage $V_{\rm out}$. The conventional COT control loop regulates the same output voltage needed to generate more on-time pulses, which leads to increase in switching loss. Thus, CFCOT control is suitable for a wide range of the output voltage.

Fig. 7 shows the experimental results of the switching frequency versus the input voltage $V_{\rm in}$ for CFCOT at operating conditions of 3.3 V output voltage $V_{\rm out}$ and 0.1 A output load $I_{\rm out}$ to measure the switching frequency from 4 to 21 V input voltage $V_{\rm in}$. When the resistor R_1 is equal to 510 k Ω to connect between the $V_{\rm in}$ and the TON pin, the switching frequency is 255 kHz, regardless of changes in $V_{\rm in}$. If the resistor R_1 is reduced to 320 k Ω , the switching frequency changes from 255 to 444 kHz and the resistor R_1 directly affects the on-time width. Between the resistor R_1 and the switching frequency are the inverse relationships.



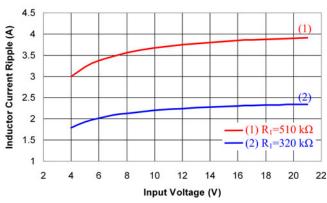


Fig. 8. Experimental results of the inductor current ripple versus the input voltage for CFCOT.

Fig. 8 shows the experimental results of the inductor current ripple versus the input voltage $V_{\rm in}$ for CFCOT at operating conditions of 3.3 V output voltage $V_{\rm out}$ and 0.1 A output load $I_{\rm out}$ to measure the inductor current ripple from 4 to 21 V input voltage $V_{\rm in}$. The blue curve of the resistor R_1 is 320 k Ω , whereas the red curve of the resistor R_1 is 510 k Ω . If the inductance is invariant, then the current ripple inductor is related to the voltage droop between the input voltage and the output voltage, which also depends on the width of on-time through (3). By substituting (2) into (3), the inductor current ripple is obtained (4). The inductor current ripple increases as the input voltage increased. Hence, it does not maintain a constant value. When the resistor R_1 is increased from 320 to 510 k Ω , the width of on-time has also increased, resulting in a larger inductor current ripple

$$\Delta I_L = \frac{V_{\rm in} - V_{\rm out}}{L} \times T_{\rm ON} \tag{3}$$

$$\Delta I_L = \frac{V_{\text{out}} \left(1 - \left(V_{\text{out}} / V_{\text{in}} \right) \right)}{I_L} \times T_S. \tag{4}$$

III. CONVENTIONAL QUICK RESPONSE CIRCUIT OF RBCOT WITH VIC RIPPLE

Two types of improved transient response circuits are typically used, namely, internal fixed by IC design [32], [33], and external setting by component or voltage source [34]. The internal fixed by IC design usually uses the feedback voltage $V_{\rm fb}$ to trigger the quick response function, which can provide a long on-time width to control the driver circuit. However, the generator circuit of quick response has a very similar on-time generator circuit. Therefore, it can use two generator circuits or just one generator circuit for on-time implementation with the internal fixed quick response, as shown in Fig. 9.

The internal fixed quick response circuit needs to add a voltage source $V_{\rm ref2}$. The $V_{\rm ref2}$ is usually designed at 80% to 90% of $V_{\rm ref}$ to prevent the occurrence of under voltage protection. If the feedback voltage $V_{\rm fb}$ is lower than $V_{\rm ref2}$, the output signal of the

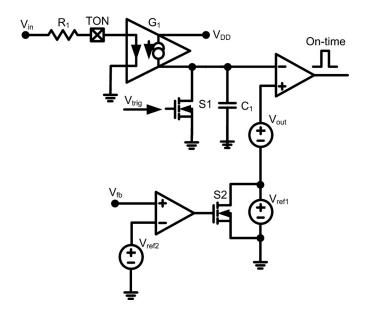


Fig. 9. One generator circuit for on-time implementation with the internal fixed quick response.

comparator changes from high level to low level signal, which can turn OFF the switch of S2. The voltage source $V_{\rm ref1}$ is set in a series connection with $V_{\rm out}$ to increase the on-time width. $V_{\rm ref1}$ is considered the maximum duty cycle limited. If $V_{\rm ref1}$ is too large, it may cause these components to suffer damage.

The main advantage of this process is that no extra pin in the IC is needed to achieve the quick response function. However, the design of the internal fixed quick response circuit can generate just one form of a long on-time width. Thus, this circuit cannot dynamically change the on-time width during different load conditions. On the other hand, the hysteresis of the comparator is difficult to design, especially for a very fast load transient, because if the hysteresis of the comparator is too small, it can induce the system to erroneously trigger a long on-time width, thereby causing high output voltage. Conversely, if the hysteresis of the comparator is too large, it can also render the quick response function unavailable.

Fig. 10 shows the external setting of the quick response ontime generator circuit. The operation principle of the external setting quick response circuit requires the addition of a voltage source $V_{\rm QRSET}$ to determine the width of QR-time. $V_{\rm QRSET}$ is connected to the QRSET pin. If the QR-time needs a long on-time width, $V_{\rm QRSET}$ should be larger than $V_{\rm out}$.

The QR trigger circuit samples the output voltage $V_{\rm out}$ and uses the low-pass filter to cause the $V_{\rm out}$ signal delay and the dc source of voltage signal $V_{\rm QRTH}$. In the steady-state operation, the output voltage droop cannot trigger the QR-time. When this abrupt voltage droop is lower than the voltage signal $V_{\rm QRTH}$, the QR trigger circuit generates a low level signal to turn OFF the switch of S2 [34]. The frequency of the low-pass filter for $R_{\rm LOW}$ and $C_{\rm LOW}$ should be much smaller than the switching frequency because the output voltage ripple may cause this system to fail in its operation with QR-time. The $V_{\rm QRTH}$ signal can be designed in IC or set by the user from the QRTH pin [34].

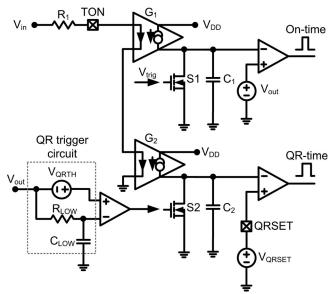


Fig. 10. External setting quick response of on-time generator circuit.

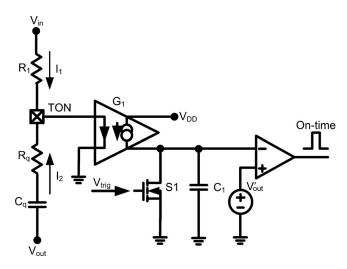


Fig. 11. Novel quick response of on-time generator circuit.

The main advantage of the external setting quick response circuit can depend on the load conditions to design the $V_{\rm QRSET}$ value generating a suitable QR time in this system. However, this method requires two extra IC pins to achieve the quick response function.

IV. NOVEL QUICK RESPONSE CIRCUIT OF RBCOT WITH VIC RIPPLE

A novel quick response of RBCOT circuit with VIC ripple for Buck converter is proposed in this paper, as well as a novel quick response of on-time generator circuit, as shown in Fig. 11. An external setting device is used to design these components, instead of a set-up voltage source. This novel quick response circuit does not require an extra pin to achieve the quick response function of IC. The system consists of a series of the resistor R_q and the capacitor C_q that are connected between the output voltage $V_{\rm out}$ and the TON pin. It operates under the principle that the high-pass filter filters high-frequency signal to pass from

 $V_{\rm out}$ to the TON pin by (5). However, the frequency of the highpass filter must be larger than or equal the switching frequency so the steady-state operation of the system is not affected. On the other hand, the user may base the design of the resistor R_q and the capacitor C_q on the worst-case operation (maximum load step).

 V_{out}' determines the peak voltage of the capacitor C_1 . Thus, if V_{out}' is high, the peak voltage increases, which causes a long ontime width. V_{out}' is implemented to provide a rippleless voltage because it can keep the switching frequency constant without causing of output voltage ripple and noise interference. V_{out}' is implemented to sample the phase voltage through a second-order low-pass filter to produce a similar V_{out} signal. Therefore, V_{out}' is rippleless and has lower transient response than the V_{out} signal

$$F_{RC} = \frac{1}{2\pi \cdot R_q \cdot C_q} \ge F_S. \tag{5}$$

When light load quickly transforms to heavy load, $V_{\rm out}$ momentarily drops through the coupling by the capacitor C_q , which induces the resistor R_q to cause a voltage droop. The voltage droop of R_q will form a current of I_2 . Thus, the resistor R_q needs to be designed first because the current of I_2 can directly change the width of on-time. However, a longer width of on-time induces the converter to deliver more energy from the input terminal to the output load. If the resistor R_q has reduced, the width of on-time becomes longer. The capacitor of C_q should be designed with the frequency of the high-pass filter. The calculation of the Laplace transform formula is shown in (6)

$$T_{\text{ON}(s)} = \frac{C_1}{G_1 \cdot \left(\frac{V_{\text{in}}}{R_1} + \frac{s \cdot C_q \cdot V_{\text{out}}}{1 + s \cdot C_q \cdot R_q}\right)} \cdot V'_{\text{out}}.$$
 (6)

The advantages of the novel quick response circuit are as follows: 1) It clearly generates a longer width of on-time that is proportional to the output voltage droop; 2) Adaption to the width of on-time depends on the load conditions of the system; 3) It only uses one generator circuit; thus, it is very convenient to design and to apply; 4) It does not require an extra pin to achieve the quick response function of IC.

V. EXPERIMENTAL VERIFICATION

The experimental results are shown to prove the feasibility and performance of this novel quick response of RBCOT circuit with VIC ripple for Buck converter. The specifications are as follows:

- 1) input dc voltage $V_{\rm in}$: 12 V;
- 2) output dc voltage V_{out} 3.3 V;
- 3) maximum output load I_{out} : 18 A;
- 4) switching frequency F_S : 255 kHz;
- 5) MOSFET S1, S2: BSC0909NS \times 2;
- 6) feedback resistors R_{d1} , R_{d2} : 68 k Ω , 12 k Ω ;
- 7) main inductor L: IHLP4040DZER1R0MA1 (1 μ H);
- 8) output capacitors C_O : 22 μ F/ 25 V (R_{CO} : 3 m Ω) × 13;
- 9) reference voltage V_{ref} : 0.5 V;
- 10) novel quick response circuit: $G_1=1(A/A); R_1=510 \text{ k}\Omega;$ $C_1=7.06 \text{ pF}; R_q=510 \Omega; C_q=390 \text{ pF}.$

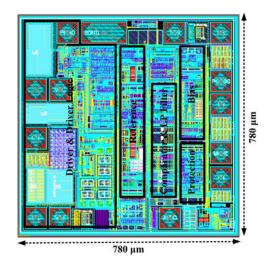


Fig. 12. Chip layout of the control IC.

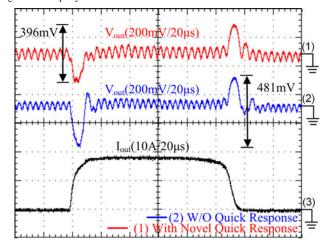


Fig. 13. Comparison of the experimental results at the load transient for the novel quick response and the no quick response.

Fig. 12 shows the chip layout of the control IC, in which the low-pass filter of the virtual inductor current ripple occupies the area marked by the LP Filter with a die size of 780 μ m \times 780 μ m.

Fig. 13 shows a comparison of the experimental results at the load transient for the novel quick response (see Fig. 10) and the no quick response (see Fig. 4). The blue waveform represents the no quick response for the output voltage signal, whereas the red waveform represents the novel quick response for the output voltage signal. The output voltage signals are measured based on the same output load, such as the black waveform. The output load is used as a function generator signal to control the switch of MOSFET to implement the load transient, which is faster than the electronics load as shown in Fig. 14.

 $V_{\rm out}$ at the load transient with the novel quick response is 396 mV and $V_{\rm out}$ at the load transient with no quick response is 481 mV. Thus, $V_{\rm out}$ with the novel quick response is lower by 85 mV than the no quick response, which is useful to prevent the $V_{\rm out}$ from dropping markedly.

Fig. 15 shows a comparison of the experimental results at the droop for the novel quick response and the no quick response.

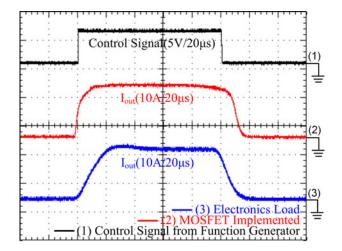


Fig. 14. Comparison of the slew rate at the load transient for the electronics load and the MOSFET implemented with a function generator signal.

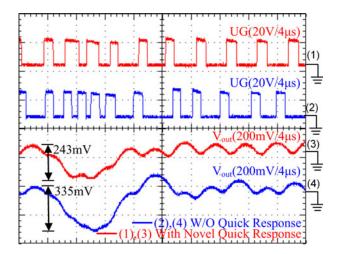


Fig. 15. Comparison of the experimental results at the droop for the novel quick response and the no quick response.

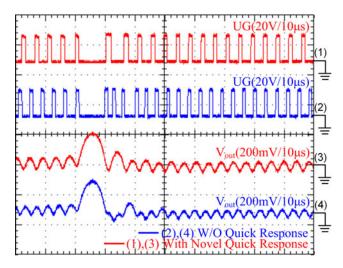


Fig. 16. Comparison of the experimental results at the load release for the novel quick response and the no quick response.

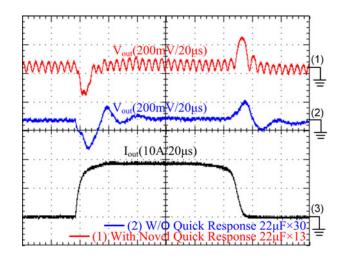


Fig. 17. Comparison of the experimental results at the load transient for the novel quick response and the no quick response.

The blue waveforms represent the no quick response for the output voltage and the UG signal, whereas the red waveforms represent the novel quick response for the output voltage and the UG signal, whose signals are measured based on the same output load.

 $V_{\rm out}$ at the droop with the novel quick response is lower than the no quick response, with a difference of about 92 mV. The setting time with the novel quick response at the droop is faster than the no quick response.

On the other hand, the UG signal with the novel quick response is obviously longer than the no quick response at the droop, which enables the input power to deliver more energy to the output terminal.

Fig. 16 shows a comparison of the experimental results at the load release for the novel quick response and the no quick response. The blue waveforms represent the no quick response for the output voltage and the UG signal, whereas the red waveforms represent the novel quick response for the output voltage and the UG signal, whose signals are measured based on the same output load. $V_{\rm out}$ at the load release with the novel quick response varies closely with the no quick response. The transient response at the load release is faster than the no quick response because $V_{\rm out}$ does not suffer a voltage droop after load release.

To further understand the advantage and superiority of this novel quick response, this paper plans based the same $V_{\rm out}$ droop with the novel quick response on to increase additional 22 $\mu {\rm F}$ of ceramic output capacitors with the no quick response. The conditions are as follows:

Condition 1: The novel quick response circuit:

- 1) output capacitors C_O : 22 μ F/ 25 V (R_{CO} : 3 m Ω) × 13;
- 2) novel quick response circuit: $G_1=1(A/A); R_1=510 \text{ k}\Omega;$ $C_1=7.06 \text{ pF}; R_q=510 \Omega; C_q=390 \text{ pF}.$

Condition 2: The no quick response circuit.

1) Output capacitors C_O : 22 μ F/ 25 V (R_{CO} : 3 m Ω) × 30.

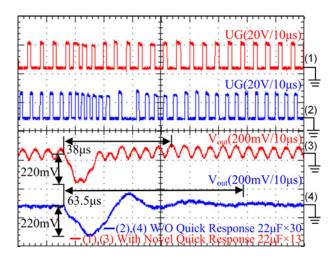


Fig. 18. Comparison of the experimental results at the droop for the novel quick response and the no quick response.

Fig. 17 shows a comparison of the experimental results at the load transient for the novel quick response and the no quick response. The blue waveform represents the no quick response with $30 \times 22~\mu\mathrm{F}$ ceramic output capacitors for the output voltage signal, whereas the red waveform represents the novel quick response with $13 \times 22~\mu\mathrm{F}$ ceramic output capacitors for the output voltage signal, whose signals are measured based on the same output load.

Based on the same $V_{\rm out}$ droop with the novel quick response, the no quick response needs to increase additional $17 \times 22~\mu{\rm F}$ of ceramic output capacitors. Thus, the novel quick response can save $17 \times 22~\mu{\rm F}$ ceramic output capacitors regardless of the cost and size of the output capacitors, both of which are the very benefits of the circuit design.

Fig. 18 shows a comparison of the experimental results at the droop for the novel quick response and the no quick response. The blue waveforms represent the no quick response with 30 \times 22 μF ceramic output capacitors for the output voltage and the UG signal, whereas the red waveforms represent the novel quick response with 13 \times 22 μF ceramic output capacitors for the output voltage and the UG signal, whose signals are measured based on the same output load.

The setting time with the novel quick response is 38 μ s, which is faster by 25.5 μ s than the no quick response at the droop. Thus, the large output capacitors can hold the $V_{\rm out}$ droop and induce the $V_{\rm out}$ ripple small. However, it may cause the system to obtain a slow transient response.

Fig. 19 shows a comparison of the experimental results at the load release for the novel quick response and the no quick response. The blue waveforms represent the no quick response with 30 \times 22 μF ceramic output capacitors for the output voltage and the UG signal, whereas the red waveforms represent the novel quick response with 13 \times 22 μF ceramic output capacitors for the output voltage and the UG signal, whose signals are measured based on the same output load.

Thus, the large output capacitors can reduce the peak voltage of $V_{\rm out}$ at the load release, but the cost and size of the output

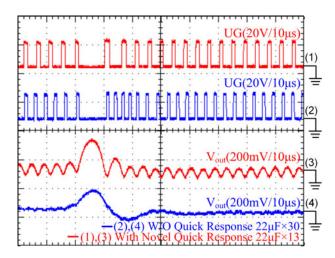


Fig. 19. Comparison of the experimental results at the load release for the novel quick response and the no quick response.

capacitors need to be sacrificed. On the other hand, the large output capacitors induce the system loop response slowly. The setting time at load release with the novel quick response is faster than the no quick response.

VI. CONCLUSION

This paper is proposed a novel quick response of RBCOT with VIC ripple for Buck converter. Using the capacitor and the resistor in a series to filter out the output voltage at load transient to dynamically change the width of on-time, the input power delivers more energy to the output terminal to prevent $V_{\rm out}$ from dropping markedly.

Experimental verifications confirm the reduction in cost and size of the ceramic output capacitors and the increase in transient response. Moreover, the proposed quick response circuit has a very simple structure and design. It is available and useful in RBCOT with VIC ripple for Buck converter.

REFERENCES

- [1] C. J. Chen, D. Chen, C. W. Tseng, C. T. Tseng, Y. W. Chang, and K. C. Wang, "A novel ripple-based constant on-time control with virtual inductor current ripple for buck converter with ceramic output capacitors," in *Proc. IEEE Appl. Energy Convers. Cong. Expo. Conf.*, Sep. 2011, pp. 1244–1250.
- [2] L. E. Gallaher, "Current regulator with AC and DC feedback," U.S. Patent 3 350 628, Oct. 31, 1967.
- [3] A. D. Schoenfeld and Y. Yu, "ASDTIC control and standardized interface circuits applied to buck, parallel and buck-boost DC-to-DC power converters," NASA, Washington, DC, NASA Rep. NASA CR-121106, Feb. 1973.
- [4] C. W. Deisch, "Switching control method changes power converter into a current source," in *Proc. IEEE Power Electron. Spec. Conf.*, 1978, pp. 300– 306.
- [5] P. L. Hunter, "Converter circuit and method having fast responding current balance and limiting," U.S. Patent 4 002 963, Nov. 1, 1977.
- [6] L. H. Dixon, "Average current-mode control of switching power supplies," in *Proc. Unitrode Power Supply Des. Semin. Handbook*, 1990, pp. 5.1–5.14.
- [7] N. Mohan, "Power electronics circuits: An overview," in *Proc. IEEE Ind. Electron. Soc. Conf.*, Oct. 1988, pp. 522–527.
- [8] N. Mohan, W. P. Robbins, P. Imbertson, T. M. Undeland, R. C. Panaitescu, A. K. Jain, P. Jose, and T. Begalke, "Restructuring of first courses in power

- electronics and electric drives that integrates digital control," *IEEE Trans. Power Electron.*, vol. 18, pp. 429–437, Jan. 2003.
- [9] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching-converter power states," in *Proc. IEEE Power Electron. Spec. Conf.*, 1976, p. 18.
- [10] D. Y. Chen, H. A. Owen, and T. G. Wilson, "Computer Aided design and graphics applied to the study of inductor-energy-storage dc-to-dc electronic power converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-9, no. 4, pp. 585–597, Nov. 1973.
- [11] P. Burger, "Analysis of a class of pulse modulated dc-to-dc power converters," *IEEE Trans. Ind. Elect. Contr. Instrum.*, vol. IECI-22, no. 2, pp. 104–116, May 1975.
- [12] C. Ni and T. Tetsuo, "Adaptive constant on-time (D-CAPTM) control study in notebook applications," Texas Instruments, Dallas, TX, Appl. Rep. SLVA281B, Jul. 2007.
- [13] R. Redl and J. Sun, "Ripple-based control of switching regulators: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.
- [14] J. Li, "Current-mode control: Modeling and its digital application," Ph.D. thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, 2009.
- [15] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.
- [16] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2001, pp. 273–279.
- [17] J. Li and F. C. Lee, "Modeling of V2 current-mode control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 298–304.
- [18] Z. Yang, S. Ye, and Y. F. Liu, "A new resonant gate drive circuit for synchronous buck converter," in *Proc. IEEE Trans. Power Electron.*, vol. 22, no. 4, Jul. 2007, pp. 1311–1320.
- [19] H. Fujita, "A resonant gate-drive circuit capable of high-frequency, and high-efficiency operation," in *Proc. IEEE Trans. Power Electron.*, vol. 25, no. 4, Apr. 2010, pp. 962–969.
- [20] W. Eberle, Z. Zhang, Y. F. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," in *Proc. IEEE Trans. Power Electron.*, vol. 24, no. 3, Mar. 2009, pp. 700–713.
- [21] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," in *Proc. IEEE Trans. Power Electron.*, vol. 21, no. 2, Mar. 2004, pp. 310–319.
- [22] X. Zhou, Z. Liang, and A. Huang, "A new resonant gate driver for switching loss reduction of high side switch in buck converter," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2010, pp. 1477–1481.
- [23] (2009). "TPS54325: 4.5 V to 18 V Input, 3 A Synchronous Step Down SWIFTTM Converter with D-CAP2TM Mode," [Online]. Available: http://www.ti.com/.
- [24] S. J. Wang, Y. H. Lee, Y. C. Lai, and K. H. Chen, "Quadratic differential and integration technique in V2 control buck converter with small ESR capacitor," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2009, pp. 211–214.
- [25] R. Redl and G. Reizik, "Switched noise filter for the buck converter using the output ripple as the PWM ramp," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2005, pp. 918–924.
- [26] R. Redl and T. Schiff, "A new family of enhanced ripple regulators for power-management applications," in *Proc. Int. Exhibition Conf. Eur.*, Nuremburg, Germany, 2008, pp. 255–268.
- [27] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.
- [28] K. D. T. Ngo, S. K. Mishra, and M. Walters, "Synthetic-ripple modulator for synchronous buck converter," in *Proc. IEEE Power Electron.*, vol. 3, no. 4, pp. 148–151, Dec. 2005.
- [29] Y. H. Lee, S. J. Wang, and K. H. Chen, "Quadratic differential and integration technique in V² control buck converter with small ESR capacitor," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 829–838, Apr. 2010.
- [30] M. Y. Yen and P. Mok, "A constant frequency output-ripple voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits* Syst., vol. 55, no. 8, pp. 748–752, Aug. 2008.
- [31] K. Y. Cheng, F. Yu, P. Mattavelli, and F. C. Lee, "Characterization and performance comparison of digital V²-type constant on-time control for buck converters," in *Proc. IEEE Control Model. Power Electron. Conf.*, Jun. 2010, pp. 1–6.
- [32] K. P. Liu, K. C. Wang, L. P. Tai, and C. S. Cheng, "Control circuit and method for a constant on-time PWM switching converter," U.S. Patent 7 834 606 B2, Aug. 2, 2007.

- [33] K Huang, "Spring modulation with fast load-transient response for a voltage regulator," U.S. Patent 7 247 182 B2, Aug. 26, 2005.
- [34] Richtek Technology Corporation, Hsinchu City, Taiwan, "Dual output 3-Phase + 2-Phase PWM controller for CPU and GPU Core power supply," RT8885 A Datasheet, 2012.



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